Design and Optimization of Low Drop-Out (LDO) Voltage Regulator in 180nm CMOS Technology

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Abstract

Low-dropout (LDO) voltage regulators are widely used in low-power electronic systems to provide a stable supply voltage while minimizing voltage headroom and power consumption. This paper presents the design and optimization of a capacitorless Low-Dropout (LDO) Voltage Regulator implemented in a 0.18 μm CMOS technology. The proposed architecture utilizes a conventional two-stage operational transconductance amplifier (OTA) with standard Miller compensation and a PMOS pass device to achieve area-efficient voltage regulation for always-on intermediate-load electronic devices. Operating from an input supply of 2.0 V to 3.3 V, the LDO delivers a stable 1.8 V output with a low dropout voltage of 100 mV at a maximum load of 10 mA. The design is specifically optimized for systems maintaining a minimum continuous load of 1 mA, under which it achieves a phase margin of >60°. Simulation results demonstrate a unity-gain frequency (UGF) of 593 kHz, a nominal quiescent current of 198 μA, and a worst-case high-frequency Power Supply Rejection Ratio (PSRR) of 46.78 dB. Comprehensive PVT corner analysis confirms robust regulation across variations, making this architecture highly suitable for reliable, intermediate-current sensor nodes and analog sub-circuits.

Keywords: *Low-Dropout Regulator, CMOS LDO, PMOS Pass Transistor, Two-Stage OTA, Power Supply Rejection Ratio (PSRR).*

1. Introduction

Modern electronic devices, ranging from smartphones to medical implants, rely on power sources such as batteries, USB ports, and external power supplies for proper operation. However, these power sources may provide voltages that are excessive, noisy, or subject to fluctuations. A low-dropout (LDO) voltage regulator is therefore employed to provide a stable DC voltage to electronic circuits while maintaining a small difference between the input and output voltages. The dropout voltage is defined as the difference between the input voltage and nominal output voltage at which the regulator can no longer maintain proper voltage regulation. A low dropout voltage allows the regulator to operate with reduced voltage headroom, thereby reducing power dissipation, which is particularly important for battery-powered and other low-power applications [1]. In addition, stability is an important consideration in LDO design, as the regulator must maintain a stable output voltage under varying load conditions. This characteristic makes LDO regulators suitable for sensitive applications that require consistent and precise voltage regulation, such as sensor systems [1].

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While recent literature extensively covers advanced LDO topologies—such as folded compensation cascode topologies and push-pull composite power transistors—these architectures often introduce significant design complexity and area overhead. A gap remains in defining the realistic performance boundaries of conventional, standard Miller-compensated LDOs when applied to modern 180 nm nodes. This work specifically investigates the optimization of a conventional two-stage OTA architecture to balance area efficiency and adequate regulation for intermediate-load applications (1 mA to 10 mA), deliberately avoiding complex transient-enhancement circuits to prioritize design simplicity and robust nominal operation.

2. Literature Review

In a conventional LDO, a power transistor, commonly referred to as the pass transistor, is connected in series between the input and output terminals of the regulator [2]. The regulator operates through a feedback mechanism in which the output voltage is sensed and compared with a reference voltage. The resulting error signal is amplified and used to control the conduction of the pass transistor, thereby regulating the output voltage supplied to the load. Through this feedback operation, the LDO can maintain a regulated output voltage while providing a low-impedance output suitable for electronic loads.

The increasing demand for small and portable electronic devices has created a need for low-voltage operation and low quiescent current to improve battery efficiency, reduce current consumption, and extend operating lifetime [3]. The trend toward higher device density in semiconductor processes has also contributed to the requirement for lower operating voltages. As component density increases, isolation dimensions decrease, resulting in lower device breakdown voltages and consequently encouraging the development of circuits capable of operating at reduced supply voltages [4]. Therefore, advances in low-power circuit design and finer semiconductor technologies have driven LDO regulators toward lower operating voltages, accurate output regulation, and reduced quiescent current [5]. Furthermore, minimizing dropout voltage is important for maximizing the available dynamic range within a given supply voltage. As supply voltages decrease, maintaining a sufficiently low dropout voltage becomes increasingly important because the signal-to-noise ratio can be adversely affected when the supply voltage is reduced while noise levels remain relatively constant [6].

One of the major challenges in LDO design is the trade-off among several important performance parameters, including quiescent current, load-transient response, dropout voltage, power-supply rejection, loop stability, and bandwidth. Improving one performance parameter can impose constraints on others, requiring careful selection and optimization of the regulator architecture and circuit parameters. For example, research has investigated capacitorless, or “capless,” LDO architectures to eliminate the need for an additional load capacitor, which can occupy considerable silicon area when implemented as an integrated component [7]. Such approaches demonstrate how architectural modifications can address specific application requirements while introducing different design considerations.

Various circuit techniques have also been incorporated into different LDO building blocks to improve overall performance according to application requirements. One approach employs a folded compensation cascode topology to implement active frequency compensation rather than relying solely on external components. A pseudo-differential technique is also incorporated to reduce the voltage difference at critical circuit nodes [8]. Another approach utilizes a current-steering technique to prioritize fast transient response. In this design, a current-feedback amplifier (CFA) is implemented as a control mechanism for the pass transistor and combined with an inverting output buffer and an open-loop voltage follower. The low input impedance of the CFA contributes to the achievement of a fast transient response [9]. Other research has focused on achieving high power-supply rejection (PSR), wideband ripple filtering, and fast transient response through the use of an N-type pass transistor, charge pump,

and dual-feedback system. In this approach, the absence of a decoupling capacitor is addressed through a dual-feedback architecture consisting of high-gain and wide-bandwidth paths [10].

Existing LDO architectures exhibit distinct trade-offs between quiescent current, transient response, and stability. For instance, while buffer-impedance attenuation allows for highly stable single-pole responses and low quiescent currents, it necessitates more complex internal circuitry. Similarly, fully capacitorless designs often suffer from severe load-dependent stability issues, requiring adaptive positive feedback or dynamic biasing that increases silicon area. Therefore, this work presents the design and optimization of a CMOS LDO voltage regulator. The proposed design aims to achieve stable 1.8 V output regulation while maintaining low quiescent current, low dropout voltage, adequate loop stability, and satisfactory transient and power-supply rejection performance. The proposed LDO is designed and evaluated at the transistor level using a 0.18 μm CMOS process. DC, AC, transient, and process-voltage-temperature (PVT) corner analyses are performed to evaluate the regulator's electrical performance and robustness under different operating conditions.

3. Design

3.1 Specifications

Table 1. Table of Specification of Proposed LDO

Parameter	Value
Process Size (μm)	0.18
Input Voltage Range (V)	1.8-3.3
Output Voltage (V)	1.8
Dropout Voltage(mV)	< 200
Output Load Current (mA)	< 10
Quiescent Current (μA)	< 400
PSRR (dB)	> 45
Phase Margin	> 60°
Unity Gain Frequency (kHz)	> 500

These specifications serve as performance metrics for the proposed LDO. The key characteristics of an LDO broadly categorized into three aspects: regulation performance, quiescent current, and operating voltage [11]. These performance characteristics are often interdependent and may introduce competing design requirements, necessitating appropriate trade-offs during the design process.

The proposed LDO targets a regulated output voltage of 1.8 V, which is suitable for low-power applications requiring reduced current consumption and improved power efficiency [12]. A low dropout voltage is targeted to enable the pass transistor to maintain proper regulation with a small input-to-output voltage difference, thereby reducing unnecessary power dissipation [7]. The error amplifier is designed to provide sufficient DC gain and phase margin to achieve accurate voltage regulation and stable closed-loop operation [13]. In addition, sufficient amplifier gain contributes to improved power-supply rejection, as the loop gain of the error amplifier can enhance the regulator's ability to suppress variations in the supply voltage [14].

3.2 Architecture Selection

Several LDO architectures have been developed to address different performance requirements, including low quiescent current, fast transient response, high power-supply rejection, and stable

operation over a wide load range. The selection of appropriate architecture therefore depends on the required performance and the intended application. For the proposed design, a conventional feedback-based LDO architecture with a PMOS pass transistor was selected due to its suitability for low-voltage regulation and its relatively straightforward implementation at transistor level.

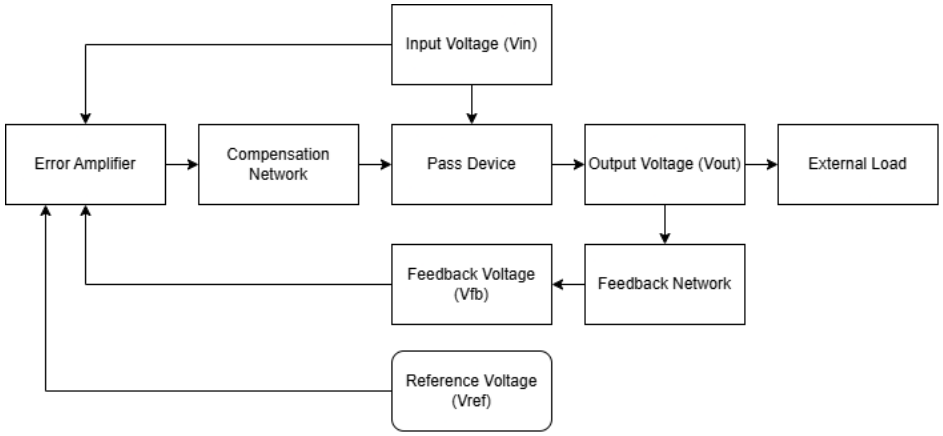


Figure 1. Block Diagram for Proposed LDO Topology

The selected architecture consists of a reference voltage, error amplifier, PMOS pass transistor, feedback network and biasing circuit as illustrated in Figure 1. The feedback voltage is compared with the reference voltage by the error amplifier, which generates a control signal to regulate the gate voltage of the PMOS pass transistor. The pass transistor subsequently adjusts the current supplied to the load to maintain the required output voltage. This feedback configuration provides a direct mechanism for regulating the output against variations in input voltage and load current.

The PMOS pass device was selected due to its suitability for low-power, low-voltage LDO applications. Compared with other pass-device configurations, the PMOS provides a low quiescent current and relatively low dropout voltage, allowing the regulator to operate with limited input-to-output voltage headroom while reducing power consumption. Although its maximum output current and speed are moderate, these characteristics are sufficient for the targeted load range of the proposed LDO. Therefore, the PMOS pass device provides a suitable balance between dropout voltage, power consumption, and load-driving capability, making it appropriate for the proposed LDO intended for small electronic devices [5].

A two-stage operational transconductance amplifier (OTA) was selected as the error amplifier to provide sufficient voltage gain for the LDO feedback loop. The OTA converts the differential voltage between the reference and feedback signals into a corresponding output current, which is subsequently used to control the pass transistor. The two-stage configuration provides high voltage gain and a high output swing, which are desirable for accurate voltage regulation and effective control of the pass device. Its high gain also strengthens the feedback loop, while the output swing allows the amplifier to provide an appropriate control voltage over the required operating range. Therefore, the two-stage OTA provides suitable error-amplifier architecture for the proposed LDO [15].

Based on these considerations, the selected architecture provides a suitable foundation for the proposed 1.8 V LDO intended for small electronic devices. The architecture and its individual circuit blocks were subsequently designed and optimized according to specifications.

3.3 Circuit Topology

Following the selection of the LDO architecture, the individual circuit blocks were designed and integrated according to the specifications established in Section 2.1. The circuit design primarily focuses

on the error amplifier, PMOS pass transistor, frequency compensation network, slew-rate enhancement circuit, and biasing circuitry. The sizing and operating conditions of these blocks were selected to achieve an appropriate balance between voltage regulation, stability, transient response, and power consumption. The complete transistor-level implementation was subsequently evaluated through iterative circuit simulations.

3.3.1 Error Amplifier

The selected two-stage OTA was implemented as the error amplifier of the proposed LDO. The transistor dimensions were selected to provide sufficient intrinsic gain and transconductance for the targeted unity-gain bandwidth while maintaining the required operating conditions. The first stage consists of a differential pair and tail current source, while the second stage provides additional voltage gain and current-driving capability for the PMOS pass transistor.

The differential-pair transistors, M1 and M3, were implemented with a width-to-length ratio of 1 µm/0.35 µm. The tail current-source transistor, M4, was sized at 4 µm/0.35 µm to establish the required bias current. For the second gain stage, the PMOS load transistor, M7, was sized at 20 µm/0.35 µm, while the NMOS gain transistor, M6, was implemented with dimensions of 5 µm/0.35 µm. The transistor dimensions were determined to provide the required amplification and drive capability for the subsequent PMOS pass stage. Figure 2 shows the schematic implementation of the proposed two-stage OTA error amplifier.

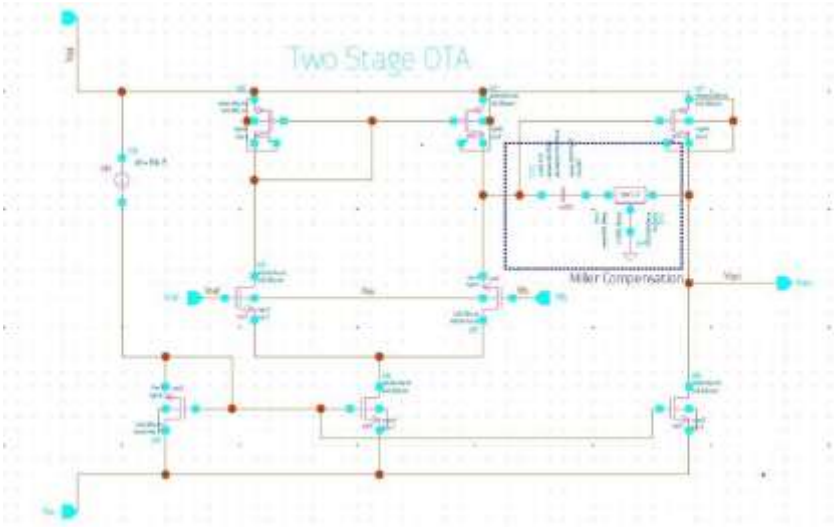


Figure 2. Two Stage OTA as Proposed Error Amplifier

3.3.2 Feedback Network

The feedback network senses the regulated output voltage and provides a scaled feedback voltage to the error amplifier. This feedback signal enables the closed-loop regulation mechanism, allowing the LDO to compensate for variations in the input supply and load current and maintain the desired output voltage [16].

The output voltage is determined by the resistor-divider ratio, as in (1).

$$V_{Out} = V_{Ref}\left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where V_{Ref} is the reference voltage, while R1 and R2 represent the upper and lower resistor of the feedback network, respectively. For the proposed LDO, a reference voltage of 1.2 V is used to obtain a nominal output voltage of 1.8 V. The feedback resistor were selected as R1 = 60 kΩ and R2 = 120 kΩ. Substitute these values into (1) gives,

$$V_{Out} = 1.2\left(\frac{60k\Omega}{120k\Omega}\right) = 1.8V \quad (2)$$

Figure 3 shows the schematic implementation of the feedback network used in the proposed LDO.

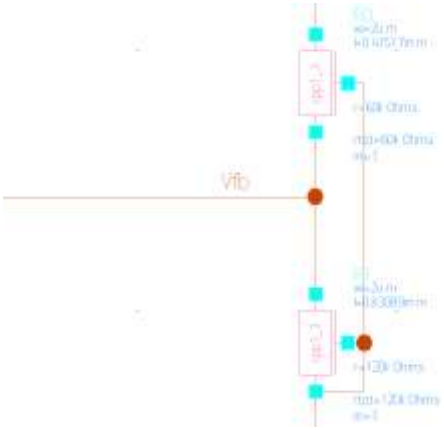


Figure 3. Resistive Divider as Proposed Feedback Network

3.3.3 Pass Device

The PMOS transistor, M29, was implemented as the main pass device of the proposed LDO to regulate the current delivered from the input supply to the output load. Its gate is driven by the output of the two-stage error amplifier, allowing the conduction of the pass transistor to be adjusted according to the difference between reference and feedback voltages [13]. When the output voltage deviates from its nominal value, the error amplifier adjusts the gate voltage of M29 to regulate the current supplied to the load and restore the output voltage.

The pass transistor was sized to provide sufficient current-driving capability for the targeted load-current range while maintaining a low dropout voltage. The final device was implemented with a total channel width of 3.6 mm and a channel length of 0.3 μm, using 18 gate fingers. The relatively large device width provides the required current-handling capability; however, the resulting parasitic capacitance at the gate and output nodes must be considered because it can affect the bandwidth and stability of the LDO. Therefore, the pass-device dimensions were considered together with the error amplifier and frequency compensation network during the circuit optimization process. Figure 4 shows the schematic implementation of the PMOS pass transistor.

The final pass-device configuration was subsequently integrated with the error amplifier, feedback network, and compensation circuit to form the complete LDO. Its ability to support the specified load-current range and maintain regulation under varying input and load conditions was evaluated through DC, AC, and transient simulations.

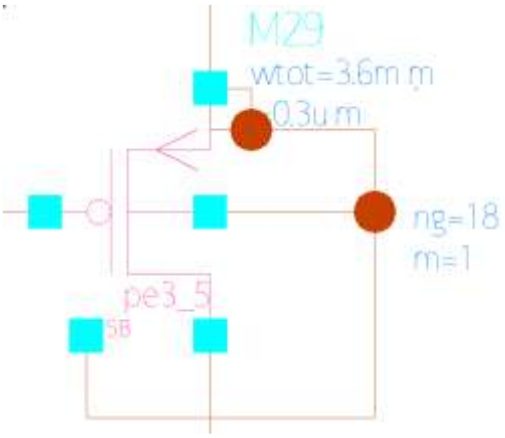


Figure 4. PMOS as proposed Pass Device

3.3.4 Current Bias Generator

The current bias generator was designed to provide a stable reference current for the error amplifier and other active circuit blocks within the proposed LDO. A self-biased beta-multiplier reference (BMR) architecture was adopted as the basis of the current-generation circuit [17]. The architecture employs transistor current mirrors to establish the feedback required for self-biasing, allowing the generated reference current to be distributed to the required branches of the LDO.

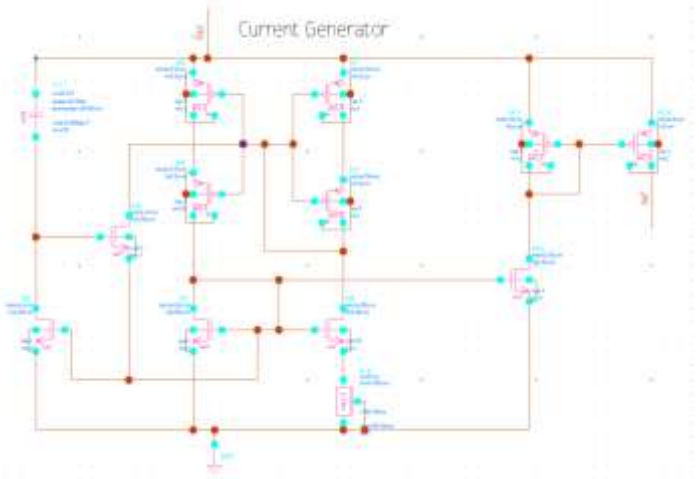


Figure 5. Proposed Bias Current Generator

The bias generator was designed to produce a reference current of approximately 30 μA as shown in Figure 5. This value was selected according to the overall quiescent-current budget of the regulator while providing sufficient biasing for the error amplifier. The operating current of the BMR is primarily determined by the transistor size ratio and degeneration resistor. The voltage difference resulting from the different current densities of the transistors establishes a voltage across the degeneration resistor, thereby determining the reference current. The resistor value and transistor dimensions were initially estimated through hand calculations and subsequently refined through simulation to obtain the targeted 30 μA current.

A start-up circuit was incorporated to ensure reliable initialization of the current-reference circuit during power-up and to prevent the BMR from settling at its zero-current operating state. The generated reference current is then mirrored to the amplifier stages and other active circuit blocks to establish their

required biasing conditions. The completed bias generator was subsequently integrated with the remaining LDO blocks for circuit-level simulation and optimization.

3.4 Simulation and Verification

The completed LDO was evaluated through transistor-level simulations using the Synopsys Custom Compiler design environment and its associated simulation tools. A series of DC, AC, transient, and power-supply rejection analyses were performed to evaluate the steady-state regulation, feedback-loop stability, dynamic response, and supply-noise rejection of the proposed design. PVT corner analysis was subsequently conducted to assess the robustness of the circuit under variations in process, supply voltage, and temperature. The simulation results were compared with the design specifications established in Section 2.1, and the circuit parameters were iteratively adjusted when the required performance was not achieved.

3.4.1 DC Analysis

DC analysis was performed to evaluate the steady-state operating characteristics of the proposed LDO and to verify its ability to maintain the required output voltage under different operating conditions. The input supply voltage and load current were varied independently to characterize the line-regulation and load-regulation performance of the regulator. The output voltage and quiescent current were monitored during the simulations to determine the steady-state response and power consumption of the LDO.

For line-regulation analysis, the input voltage was swept across the specified operating range while maintaining a fixed load condition. The resulting variation in output voltage was recorded to evaluate the ability of the LDO to maintain its nominal 1.8 V output despite changes in the input supply. The dropout behavior was also evaluated by reducing the input voltage toward the minimum operating voltage and identifying the point at which the regulator could no longer maintain the required output voltage. Similarly, Load-regulation analysis was performed by varying the load current from the minimum to the maximum specified value while maintaining a constant input voltage. The corresponding output-voltage variation was recorded to evaluate the ability of the feedback loop and PMOS pass device to maintain regulation under changing load conditions. The quiescent current was also measured under the relevant operating conditions to determine the current consumed by the LDO itself independently of the external load [2].

The DC operating points of the transistors were additionally examined to ensure that the devices operated within their intended regions. These operating-point checks were used during the design optimization process to identify unsuitable bias conditions and to ensure that the error amplifier, current-reference circuit, and PMOS pass device operated correctly before proceeding to AC and transient analysis.

3.4.2 AC / Stability Analysis

AC analysis was performed to evaluate the frequency response and closed-loop stability of the proposed LDO. The loop gain was analyzed to determine the DC gain, unity-gain frequency (UGF), and phase margin, which are important indicators of the regulation accuracy, bandwidth, and stability of the feedback system. The feedback loop was broken at an appropriate point in the LDO, and a small-signal probe was introduced to obtain the loop-gain response without significantly disturbing the original circuit operating conditions.

The resulting magnitude and phase responses were examined over the frequency range of interest. The DC loop gain was obtained from the low-frequency magnitude response, while the UGF was

identified at the frequency where the loop gain magnitude reached 0 dB. The phase margin was determined from the phase response at the corresponding unity-gain frequency. These parameters were used to assess whether the proposed compensation network provided sufficient stability while maintaining the required bandwidth [18].

The AC analysis was performed under different load-current conditions because changes in load current modify the output impedance and consequently affect the pole locations of the LDO. The compensation capacitor and nulling resistor were therefore adjusted iteratively during the optimization process to obtain an appropriate trade-off between UGF and phase margin. The final frequency response was subsequently evaluated under the specified operating conditions to verify the stability of the proposed LDO.

3.4.3 Transient Analysis

Transient analysis was performed to evaluate the dynamic response of the proposed LDO under rapid changes in load demand. A load-current step was applied between the minimum and maximum specified load conditions to simulate a sudden variation in the current drawn by the electronic load. The resulting output-voltage response was monitored to evaluate the regulator's ability to restore the nominal output voltage following the load transition.

The transient response was evaluated based on the magnitude of the output-voltage deviation, including the undershoot and overshoot, as well as the subsequent recovery of the output voltage toward its regulated value. The gate voltage of the PMOS pass transistor was also monitored to observe the response of the control loop during the load transition. These characteristics provide an indication of the response capability of the error amplifier, pass transistor, compensation network, and slew-rate enhancement circuit [6].

The load current was stepped from 1 mA to 10 mA to represent the maximum load transition specified for the proposed LDO. The simulation was performed over a sufficient time interval to capture the initial voltage deviation and subsequent recovery of the output voltage. The transient response was subsequently used to assess the effectiveness of the optimized circuit in maintaining output regulation under dynamic load conditions.

3.4.4 Power Supply Rejection Analysis

The power-supply rejection ratio (PSRR) analysis was performed to evaluate the ability of the proposed LDO to attenuate variations and disturbances from the input supply before they appear at the regulated output. A small-signal AC perturbation was applied to the input supply, and the resulting output response was monitored over the frequency range of interest. The PSRR was determined from the ratio between the input supply perturbation and the corresponding output-voltage variation.

The analysis was performed over the specified frequency range to characterize the frequency-dependent supply-noise rejection of the proposed LDO. The resulting PSRR response was examined to identify the frequencies at which the regulator provides effective supply-noise attenuation and the frequencies at which its rejection capability decreases. The influence of the feedback loop, error amplifier, and other active circuit blocks on the overall PSRR response was also considered during the circuit optimization process [2].

The simulated PSRR response was subsequently compared with the specified performance target to assess the effectiveness of the proposed LDO in suppressing supply variations. The analysis was performed at the specified operating conditions, with additional evaluations conducted where necessary to examine the effect of operating and loading conditions on the PSRR performance.

3.4.5 Process, Voltage, Temperature (PVT) Corner Verification

Process-voltage-temperature (PVT) corner analysis was performed to evaluate the robustness of the proposed LDO under variations in process technology, supply voltage, and operating temperature. The analysis was conducted after circuit optimization to determine the variation in key performance parameters under different operating conditions and to identify the corresponding worst-case performance.

Five process corners available in the adopted CMOS process were evaluated, namely typical mean (tm), worst-case one (wo), worst-case power (wp), worst-case speed (ws), and worst-case zero (wz). For each process corner, simulations were performed at three temperature conditions of −40 °C, 25 °C, and 125 °C. The input supply voltage was also varied across the specified operating range to evaluate the effect of supply-voltage variation on the regulated output and dropout behavior.

The PVT simulations were used to evaluate the variation of the principal LDO performance parameters, including output voltage, loop gain, phase margin, PSRR, and dropout voltage. For dropout-voltage verification, the input voltage was swept from 1.8 V to 3.3 V for each process-temperature combination. The minimum input voltage at which the LDO maintained the required output regulation was identified, and the corresponding dropout voltage was determined from the difference between the minimum regulating input voltage and the nominal output voltage.

The results obtained from each process and temperature combination were subsequently compared with the specified design requirements to identify the worst-case operating conditions. Particular attention was given to the output voltage and dropout voltage under supply-voltage variation, while loop gain and phase margin were examined to assess the stability of the feedback loop. PSRR was also evaluated to determine the ability of the proposed LDO to reject supply variations across the operating conditions considered.

4. Results and Discussions

The proposed LDO was evaluated through transistor-level simulation to assess its steady-state regulation, frequency response, transient behaviour, power-supply rejection, and robustness under PVT variations. The simulated results are compared with the design specifications established in Section 2.1 to determine the effectiveness of the proposed architecture and the optimization performed during the design process.

4.1 DC Performance

To determine the dropout voltage, the input voltage was swept from 1.8 V to 3.5 V while maintaining a load current of 10 mA. Figure 6 shows the variation of output voltage with respect to input voltage.

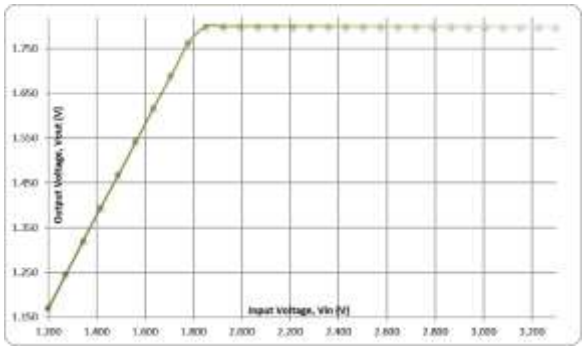


Figure 6. Output Voltage Response of Proposed LDO as Function of Input Voltage

The simulated input-voltage sweep from Figure 6 also demonstrates the regulation and dropout behavior of the proposed LDO. At low input voltages, the output voltage increases with the input voltage because insufficient voltage headroom is available across the PMOS pass device to maintain the nominal 1.8 V output. As the input voltage increases beyond the dropout region, the output voltage approaches 1.8 V and remains relatively constant over the remaining input-voltage range. This indicates that the feedback loop effectively regulates the output once sufficient headroom is available across the pass device.

Figure 7 shows the load-regulation characteristic of the proposed LDO over a load-current range of 100 μA to 10 mA. The output voltage decreases gradually as the load current increases, from 1.799152 V at 100 μA to 1.799042 V at 10 mA. This corresponds to an output-voltage variation of 0.110 mV over the evaluated load-current range. Consequently, the calculated load regulation is approximately 0.0111 mV/mA. The relatively small variation in output voltage indicates that the feedback loop effectively compensates for the increased load demand and maintains the regulated output close to the nominal 1.8 V.

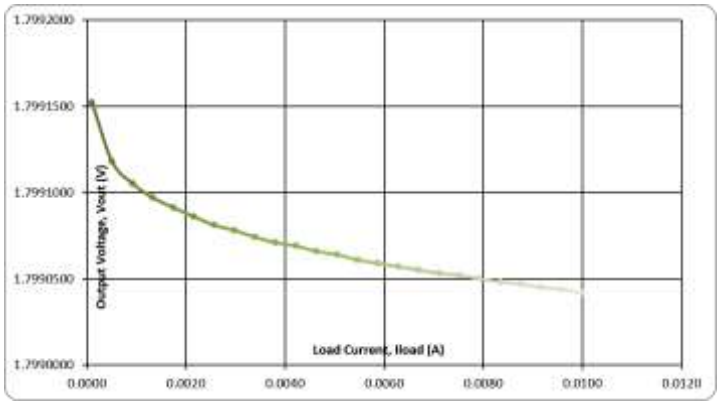


Figure 7. Output Voltage Response of Proposed LDO as Function of

4.2 AC Performance

Figure 8 shows the variation of quiescent current with input voltage. The quiescent current increases with the input voltage, ranging from approximately 109 μA at 1.2 V to approximately 199 μA at 3.3 V. A relatively sharp increase in quiescent current is observed around the transition to the regulated operating region, after which the current increases more gradually with the input voltage. At the nominal operating voltage, the quiescent current remains below 200 μA, indicating that the proposed design satisfies the targeted low-power requirement. The increase in quiescent current with input voltage is

associated with the increased bias current consumption of the active circuit blocks under higher supply voltage conditions. Table 2 summarizes the simulated performance and respective load current.

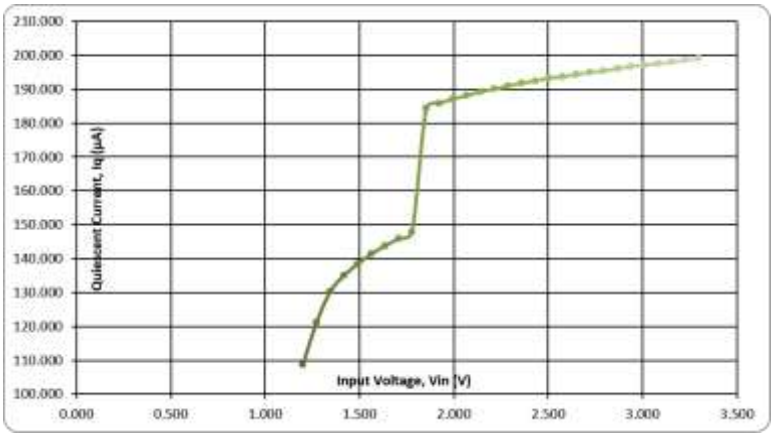


Figure 8. Quiescent Current of Proposed LDO as function of Input Voltage

4.3 Transient Performance

The transient performance of the proposed LDO was evaluated by applying repetitive load-current transitions between 1 mA and 10 mA. The corresponding output-voltage response is shown in Fig. X. When the load current increases from 1 mA to 10 mA, the output voltage exhibits a transient undershoot due to the sudden increase in load demand as depicted in Figure 9. The output voltage decreases from approximately 1.799 V to a minimum of 1.768 V, corresponding to an undershoot of approximately 31

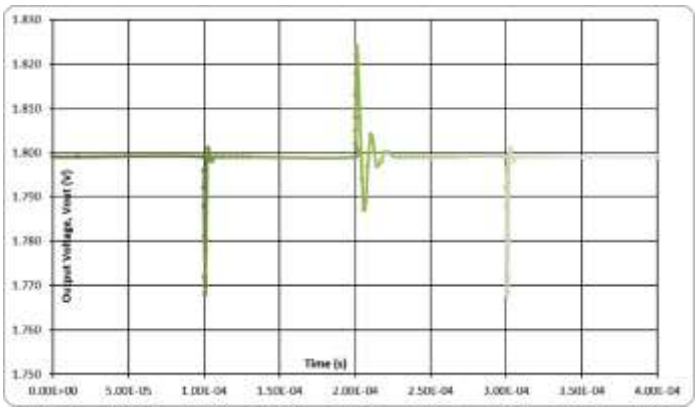


Figure 9. Transient Response of Proposed LDO

mV. The output subsequently recovers toward its nominal regulated value, reaching approximately 1.799 V within several microseconds after the load transition.

Conversely, when the load current decreases from 10 mA to 1 mA, the reduction in load demand produces an output-voltage overshoot. The output voltage reaches a maximum of approximately 1.824 V, corresponding to an overshoot of approximately 25 mV relative to the initial steady-state value of approximately 1.799 V. The output subsequently exhibits damped oscillatory behavior before returning toward the regulated output voltage. A similar response is observed for the subsequent 1 mA-to-10 mA transition at approximately 300 µs, where the output voltage again reaches a minimum of approximately 1.768 V. The LDO exhibits a maximum output slew rate of approximately 0.10 V/µs during the load transient. Using a ±1% settling criterion relative to the nominal 1.799 V output, the settling times are approximately 1.6 µs for the 1 mA-to-10 mA transition and 3.1 µs for the 10 mA-to-1 mA transition.

The observed transient deviations are associated with the finite response speed of the feedback loop and the dynamic interaction between the error amplifier, PMOS pass device, compensation network, and slew-rate enhancement circuit. Nevertheless, the repeated load transitions demonstrate that the proposed LDO is able to recover its regulated output following successive changes in load demand.

4.4 Power Supply Rejection Ratio (PSRR)

Figure 10 presents the PSRR response of the proposed LDO over a frequency range from 1 Hz to 100 MHz. The regulator exhibits strong supply-noise rejection at low frequencies, with a PSRR of approximately 104.6 dB at 1 Hz. As the frequency increases, the PSRR gradually decreases, reaching approximately 53.9 dB at 100 kHz. The minimum PSRR of approximately 46.8 dB occurs at around 355 kHz, indicating reduced supply-noise rejection as the effectiveness of the feedback loop decreases with frequency. Beyond this point, the PSRR improves and reaches approximately 58.1 dB at around 4.8 MHz before gradually decreasing to approximately 50.3 dB at 100 MHz. The observed frequency-dependent response demonstrates that the proposed LDO provides strong low-frequency supply rejection, while its rejection capability becomes increasingly dependent on the high-frequency characteristics of the feedback and compensation networks.

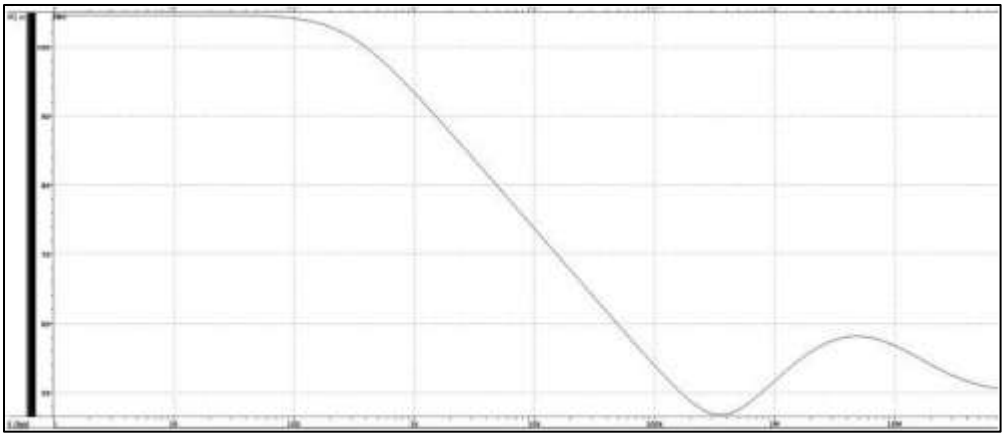


Figure 10. PSRR Performance of Proposed LDO

4.5 Process, Voltage and Temperature (PVT) Corner Verification

The robustness of the proposed LDO was evaluated through PVT corner analysis by varying the process corner, supply voltage, and temperature. Five process conditions, namely tm, wo, wp, ws, and wz, were evaluated at supply voltages of 2 V, 3.3 V, and 5 V and temperatures of −40 °C, 25 °C, and 125 °C. Table 3 summarizes the resulting ranges of output voltage, quiescent current, and phase margin across the five process corners.

Table 2. Corner Verification for Output Voltage, Quiescent Current and Phase Margin

Temperature	V_{DD} (V)	Output Voltage Range (V)	Quiescent Current Range (μA)	Phase Margin Range (°)
-40	2.0	1.79919–1.79993	132.39–194.61	69.66–72.64
	3.3	1.79929–1.79945	140.13–205.12	71.77–74.25
	5.0	1.79852–1.79870	177.83–264.69	76.30–77.96
25	2.0	1.79864–1.79887	162.89–240.10	65.72–69.58
	3.3	1.79887–1.79911	173.74–254.81	68.03–71.34
	5.0	1.79784–1.79810	213.99–317.46	71.72–74.57
125	2.0	1.79753–1.79882	211.90–307.45	61.39–66.42
	3.3	1.79812–1.79863	230.07–332.82	63.94–68.09
	5.0	1.79691–1.79848	271.74–397.36	66.34–70.29

The output voltage remains close to the nominal 1.8 V under the evaluated PVT conditions. Across all simulated combinations, the output voltage varies from 1.79691 V to 1.79993 V. The largest deviation occurs at 125 °C and 5 V, where the output voltage reaches 1.79691 V under one of the process corners. This corresponds to a deviation of approximately 3.09 mV from the nominal 1.8 V output.

The quiescent current exhibits a larger variation with supply voltage and temperature. Across all PVT conditions, the simulated quiescent current ranges from 132.39 μA to 397.36 μA. The highest quiescent current occurs at 125 °C and 5 V, indicating increased power consumption under high-temperature and high-supply conditions. This variation should be considered when assessing the low-power performance of the regulator under worst-case operating conditions.

The phase margin remains above 61° across all evaluated PVT conditions, with values ranging from 61.39° to 77.96°. The minimum phase margin occurs at 125 °C and 2 V, demonstrating that the feedback loop retains a positive stability margin even under the evaluated worst-case conditions. Overall, the PVT results demonstrate that the proposed LDO maintains regulated output voltage and adequate loop stability across the simulated process, supply-voltage, and temperature variations.

4.6 Performance Summary

Table 3. Summary of Simulated Performance of Proposed LDO

Parameter	Target Specification	Simulated Performance
Output Voltage	1.8V	1.799V
Dropout Voltage	< 200 mV	100 mV
Quiescent Current	< 400 μA	198 μA (nominal), 397.36 μA (Worst-Case PVT)
Phase Margin	> 60°	69.7° @ 10mA
Unity Gain Frequency	>500 kHz	593.23 kHz @ 10mA
Load Regulation	-	0.011 mV/mA
PSRR	> 45 dB	105 dB (DC), 46.78 dB (worst-case at 355 kHz)
Transient Undershoot	-	31 mV
Transient Overshoot	-	25mV
Increasing Load Settling Time	-	1.6 μs
Decreasing Load Settling Time	-	3.1 μs

Rising Slew Rate	-	0.05 V/μs
Falling Slew Rate	-	0.10 V/μs

Table 4 compares the performance of the proposed capacitorless LDO with several previously reported designs. The proposed regulator achieves the lowest dropout voltage of 100 mV among the selected works while maintaining a phase margin of 69.7°, indicating robust loop stability. In addition, the line regulation of 0.144 mV/V and load regulation of 20 μV/mA demonstrate effective output voltage regulation under varying supply and load conditions. Although the quiescent current of 198 μA is higher than some reported designs, the regulator achieves stable operation with only a 100 pF load capacitor, making it suitable for capacitorless applications. Overall, the results demonstrate that the proposed design provides a balanced trade-off between stability, regulation accuracy, and power consumption.

Table 4. Performance comparison of the proposed capacitorless LDO with several previously reported designs

Parameter	**[19]**	**[20]**	**[1]**	**[21]**	**This Work**
Process (nm)	350	350	180	180	180
V_{In} (V)	3.3 – 3.5	2.7 – 3.3	3.3	1.8	2 – 3.3
V_{Out} (V)	2.8	-	1.8	0.8	1.8
$V_{Dropout}$ (mV)	500	200	300	100	100
I_{Load} (mA)	50	200	100	40	10
$I_{Quiescent}$ (μA)	50	340	< 1000	-	198
C_{Load}	10 pF	100 pF	33 μF	500 fF	100 pF
Settling Time (μs)	-	-	-	0.42	25
Load Regulation (μV/mA)	310	170	< 1%	4.09	20
Line Regulation (mV/V)	23.4	2	-	800	0.144
PSRR (dB)	45 @ 100 kHz	> 45 @ (0 – 20kHz)	> 60	50.86 @ 100kHz	54 @ 100 kHz
Phase Margin (°)	57	> 65	52	66.7	69.7

5. Conclusions

This work presented the design and transistor-level simulation of a CMOS low-dropout voltage regulator intended for small electronic devices. The proposed LDO employs a PMOS pass transistor, two-stage OTA error amplifier, resistive feedback network, Miller compensation, and beta-multiplier-based bias generator. The circuit was implemented using a 0.18 μm CMOS process and evaluated through DC, AC, transient, PSRR, and PVT simulations. Under nominal operating conditions, the regulator achieved an output voltage of approximately 1.799 V, a dropout voltage of approximately 100 mV, and a quiescent current of 198 μA. The simulated load regulation was 0.011 mV/mA over the evaluated 100 μA to 10 mA load range, demonstrating good steady-state output regulation.

The transient and frequency-domain results demonstrated the dynamic characteristics and limitations of the proposed design. For a 1 mA-to-10 mA load transition, an output-voltage undershoot of approximately 31 mV was observed, while the reverse transition produced an overshoot of approximately 25 mV. The corresponding settling times based on a ±1% criterion were approximately 1.6 μs and 3.1 μs, respectively. At a 10 mA load, the loop achieved a phase margin of 69.72° and a unity-gain frequency of 593.23 kHz, although the phase margin decreased to 14.18° at 100 μA. The minimum PSRR was 46.78 dB over the evaluated frequency range. PVT analysis demonstrated that the output voltage remained within 1.79691–1.79993 V and the phase margin remained above 61° across the evaluated corners.

Overall, the proposed LDO demonstrates effective output regulation and low-dropout operation, but the simulation results also identify limitations in light-load stability, loop bandwidth, PSRR, and worst-case quiescent current. Future optimization should therefore focus on improving the low-load feedback-loop stability and bandwidth while maintaining low quiescent current and transient performance. These improvements could further enhance the suitability of the proposed LDO for low-power integrated electronic systems.

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Conflicts of interest

We declare no conflict regarding the publication of the study.

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