Development of a 5 V Multiport Switch-Mode Power Supply with an Integrated Load Indicator for Enhanced Power Reliability

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Abstract

Switch Mode Power Supplies (SMPS) have become a preferred alternative to traditional linear power supplies due to their compactness, efficiency (70-95%), compatibility with wide-range input voltage and environmental benefits. Unlike linear power supplies, which are bulky and inefficient, SMPS offers higher efficiency, smaller size, and the capability to handle varying input voltages with minimal heat generation, making it ideal for modern electronic applications. This paper presents the development of a 5V multiport switch mode power supply with integrated load indicator for enhanced power reliability using flyback converter topology, aimed at delivering a stable and efficient power source for critical applications in telecommunications, data centers, and consumer electronics. A key addition to this design is a load indicator feature, which provides an immediate visual signal if there is a disruption in power delivery, such as from a damaged cord or broken connection. If the load indicator does not light up (yellow LED), users can quickly identify issues related to faulty cables or connectors without complex troubleshooting, ensuring quick diagnostics and reliability in power delivery. The SMPS design eliminates the need for large, heat-generating components typical of linear power supplies, integrating overvoltage and overcurrent protection to safeguard both the SMPS and connected devices. Performance tests were conducted to evaluate the SMPS under varying input voltages and load conditions, ensuring compliance with international safety and performance standards. Results showed that the SMPS achieved a stable 5V output with peak efficiency of 85.2% under full load, while the load indicator feature effectively provided visual feedback on power supply status. The SMPS maintained smooth regulation over a broad input voltage range, demonstrating its adaptability to fluctuating power conditions, making it a practical, energy-conscious solution.

Keywords: *Switch Mode Power Supply (SMPS), Linear power supply, Load Indicator, Flyback converter.*

1. Introduction

A power supply is a component that every electrical gadget needs. It transforms an Alternating Current (AC) power line voltage into a constant state Direct Current (DC) output voltage. In the modern world, the demand for energy-efficient and reliable power supplies in consumer electronics has significantly increased. Traditional linear power supplies, while simple in design, suffer from poor efficiency, large size, and substantial heat generation, making them unsuitable for high-performance applications. The sustained growth of power-intensive infrastructure, including cloud-computing data centres, fifth-generation (5G) telecommunications networks, and portable consumer devices, has intensified demand for power conversion solutions that combine high efficiency, compact geometry, and robust fault-tolerance [1][2]. Consequently, there is a pressing need for a more efficient power conversion technology that can cater to the needs of modern electronic devices.

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Based on power density and efficiency, Switched Mode Power Supply (SMPS)s are more popular than linear power supplies for most contemporary applications. In this paper, the primary challenge is to design a SMPS that can provide a stable output voltage with high efficiency and minimal heat dissipation. Moreover, to further enhance reliability, this SMPS design incorporates a load indicator feature that provides immediate visual feedback on power continuity. If a connection issue, such as a damaged cord, interrupts power flow to the load, the unlit indicator (yellow LED) helps users quickly identify and resolve faults without complex troubleshooting.

A SMPS is a power electronics topology, which consists of two power stages. The AC supply is converted to DC in the first stage, and the DC voltage is then changed to the intended DC output voltage in the second stage. There are several topologies used in SMPS like push-pull topology (AC-DC converter for high power applications), buck-boost (DC-DC converter) and also flyback topology [3]. Each type of converter offers unique advantages and is tailored to specific applications. In this paper, the flyback converter topology is chosen because it is particularly beneficial for applications requiring electrical isolation. This converter naturally provides electrical isolation between the input and output due to its transformer-based design. Such isolation is crucial for safety, especially in phone chargers connected to high-voltage mains supplies, as it helps protect both the user and the device from potential faults or power surges. It is widely used in low-power applications (5W – 150W) and operates at relatively high frequencies [3], typically in the range of 15–50 kHz. This higher operating frequency increases its efficiency compared to traditional linear power supplies, which operate at much lower frequencies, typically 50–60 Hz. Its main features are simplicity, low cost, and galvanic isolation [4]. Recent investigations have demonstrated that flyback converters can achieve efficiencies exceeding 85% through quasi-resonant switching [5] and passive circuit optimisation [6], affirming the topology's continued relevance in state-of-the-art designs. The novelty of this study lies in the simultaneous integration of a load indicator circuit within a 5V multiport flyback-based SMPS, enabling real-time visual feedback on power delivery continuity without requiring specialised diagnostic equipment. While prior works have investigated flyback converter efficiency and protection mechanisms independently, the present work uniquely unifies high-efficiency power conversion (peak 85.2%) with an embedded fault-detection mechanism.

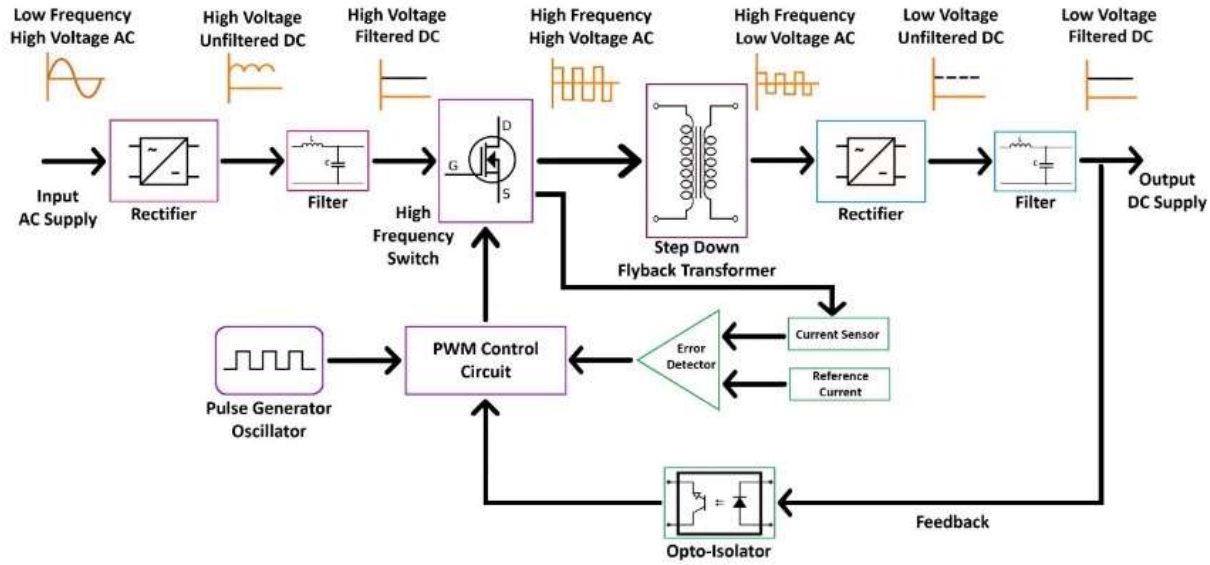


Figure 1: Typical SMPS block diagram

The aim of this study is to design and develop a 5V multiport Switch Mode Power Supply (SMPS) using a flyback converter topology with an integrated load indicator circuit for real-time power delivery monitoring, by detailing the design and component selection methodology, demonstrating the integration and operation of the load indicator circuit, and evaluating the prototype's performance under both single and full load conditions across a universal input voltage range of 85V–265V AC.

Advances in wide-bandgap semiconductor devices have significantly improved flyback converter performance. Gallium nitride (GaN) MOSFETs used in flyback configurations have enabled switching frequencies exceeding 1 MHz while reducing switching losses, with reported conversion efficiencies above 90% in compact adapter designs [7]. Despite these advantages, the relatively high cost of GaN devices continues to limit their adoption in cost-sensitive applications. Consequently, silicon-based implementations employing optimised PWM controllers such as the UC3843 remain a practical and economical solution for low-power SMPS designs [8]. In addition, a simple passive switching-loss reduction circuit consisting of a diode, an inductor, and an auxiliary transformer winding has been shown to improve flyback converter efficiency to approximately 93.5% [6]. Quasi-resonant switching techniques have also been reported to provide further efficiency improvements in low-power flyback converters.

2. Design methodology

The flyback converter is a popular topology used for low-power applications due to its inherent ability to provide electrical isolation and efficient power conversion. The operation of a flyback converter is simple; energy is absorbed into the primary winding L_p, when the switch is switched on, and after the switch is turned off, the stored energy is transferred to the secondary winding L_s [9].

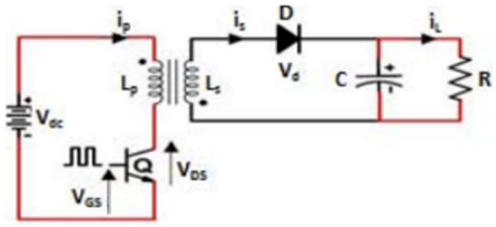


Figure 2: Switch turn-on

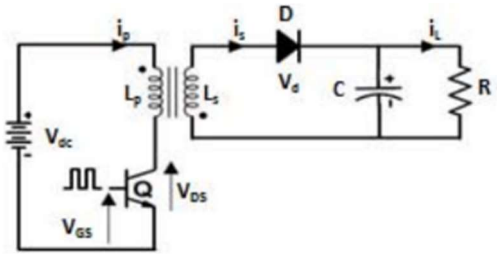


Figure 3: Simplified flyback converter

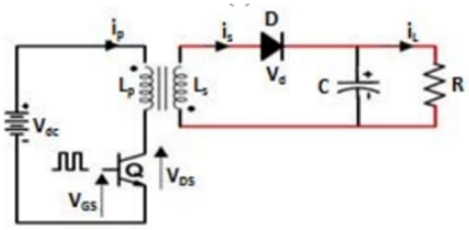


Figure 4: Switch turn-off

L_p - L_s are merely coupled inductors, indicating the absence of transformer action. When switch Q is activated, the primary winding receives V_{dc}. Primary current i_p increases linearly to its highest value due to constant V_{dc}. L_s and the primary inductor, and hence the diode, D, are oppositely polarized at this point [10]. According to Figure 2, the capacitor C supplies the load current. When switch Q is deactivated, stored energy at the air gap and magnetic core are transferred to secondary winding and load is fed by inductor L_s . I_s discharge linearly over resistive load. Stored energy at the air gap can be obtained from primary inductance and primary current by equation (1).

$$E = \frac{1}{2} \times L_p \times i_p^2 \quad (1)$$

Step-by-step design procedure:

i. Define output specifications: Vout = 5V DC, Iout = 4A, Pout = 20W.
ii. Select topology: flyback converter for galvanic isolation and multi-port capability.
iii. Specify universal input range: 85–265V AC (IEC 62368-1 compliant).
iv. Design input stage: EMI filter, NTC thermistor, bridge rectifier, bulk capacitor.
v. Design switching stage: UC3843 PWM controller at 47 kHz, MOSFET selection.
vi. Design isolation transformer: turn ratio, primary inductance, ETD29 core.
vii. Design secondary-side rectification and output filtering.
viii. Design feedback network: TL431 shunt regulator and PC817 optocoupler.
ix. Integrate load indicator sub-circuit: BC547 transistor, LED, current-limiting resistor.
x. Prototype construction, load testing, and efficiency calculation at 7 input voltage levels.

Table 1 Design specification

Input Voltage range	85V - 265V AC (Universal input)
Switching Frequency	47kHz
Output Power	20W
Estimated Efficiency	85%
Output Voltage	5V DC
Output Current	4A
Regulation	±5%

2.1. Input stage

To guarantee the stability, effectiveness, and safety of the power supply unit, the input stage of a SMPS is essential. The SMPS is protected, and optimal performance is ensured by key components in the input stage, which are commonly an Electromagnetic Interference Filter (EMI filter), a Negative Temperature Coefficient (NTC) thermistor, and a fuse.

2.1.1. Input fuse selection

Input Voltage Range: 85V to 265V AC
Maximum Input Power: 25W (> 80% efficiency).
Maximum Input Voltage ($V_{in,min}$): 85V AC. Assuming a Power Factor (PF) of 0.9
Input Current (I_{in}):

$$I_{in} = \frac{P_{in}}{V_{in,min} \times Power\ factor\ (PF)} = \frac{25W}{85V \times 0.9} \approx 0.327 \quad (2)$$

To choose the fuse, consider a fuse rating of 1.5 to 2 times the maximum input current to account for inrush current and provide some margin:

I_{fuse} = 2 × 0.327A ≈ 0.65A

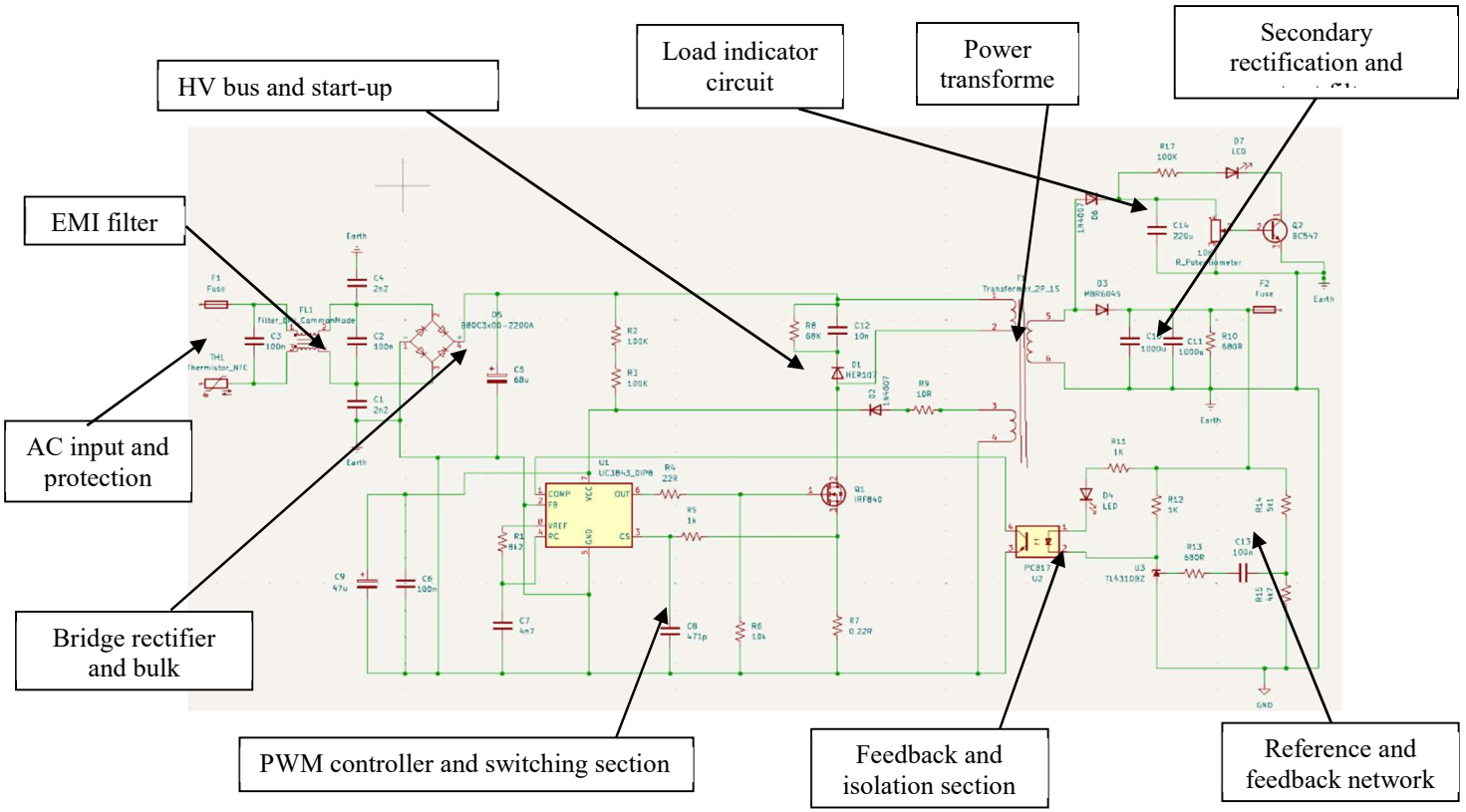


Figure 5: Flyback converter circuit diagram

2.1.2. Bridge rectifier selection

Input Voltage Range**:** 85V to 265V AC
Peak Input Voltage (V_{peak})

$$V_{peak} = V_{in,max} \times \sqrt{2} = 265V \times 1.414 \approx 374V \quad (3)$$

The rectified DC voltage is approximately equal to the peak input voltage
Rectifier Current Rating: The rectifier should handle the Root Mean Square (RMS) input current

$$I_{rect} = 1.5 \times I_{in} \approx 1.5 \times 0.327A \approx 0.5A \quad (4)$$

Considering inrush current and other transients, a 1A or 2A bridge rectifier would be sufficient.

2.1.3. Bulk capacitor selection

The capacitance is determined by the ripple voltage you can tolerate at the input, typically set between 5% to 15% of the DC voltage. Given the rectified DC voltage of around 374V:

$\Delta V_{ripple} \approx 15\% \times 374V \approx 56V$

The capacitance required to limit the ripple voltage can be estimated as:

$$C_{bulk} = \frac{I_{load}}{2 \times f \times \Delta V_{ripple}} \quad (5)$$

Where:

I_{load} is the average input current

f is the line frequency (50Hz or 60Hz).

For a 50Hz supply:

$$C_{bulk} = \frac{0.327A}{2 \times 50Hz \times 56V} \approx 58\mu F$$

2.2 UC3843 PWM IC

The UC3843 IC is a current Mode Pulse Width Modulation (PWM) Controller, widely used in power supply designs. It operates at a fixed frequency determined by an external timing capacitor and resistor, providing flexibility in setting the switching frequency, which can range from tens to hundreds of kHz. The UC3843 was selected for its low-voltage application suitability, 8.5V UVLO (Under-Voltage Lockout) turn-on threshold, 7.6V UVLO turn-off threshold, and peak-current control mode, which are well suited to flyback designs [8].

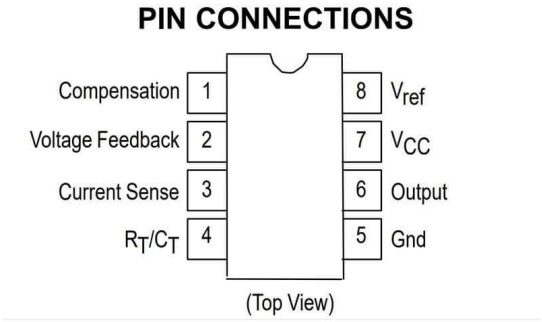


Figure 6: UC3843 IC

2.2.1 Oscillation components (Timing resistor and capacitor)

The UC3843 sets the switching frequency using an external resistor R_T and capacitor C_T connected to the R_T/C_T pin. The switching frequency is crucial for the converter's performance and is given as 47kHz in the specifications.

The switching frequency f_s for the UC3843 is determined by the formula:

$$f_s = \frac{1.72}{R_T \times C_T} \tag{6}$$

To achieve the target switching frequency f_s of 47kHz:
Timing capacitor selection: A typical value for C_T is between 1nF to 10nF. Choosing C_T to be 4.7nF
The timing resistor R_T calculation
Substituting f_s = 47kHz and $C_T = 4.7nF$ into the frequency formula

$$R_T = \frac{1.72}{47kHz \times 4.7nF}$$

$$R_T \approx 8.2\text{k}\Omega$$

Thus, R_T is approximately 8.2kΩ and C_T is 4.7nF to achieve the desired switching frequency of 47kHz.

2.2.2. Current sensing components

The current sensing resistor is placed in the source path of the Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) to provide feedback on the current through the primary winding of the transformer. Selecting Current Sensing Resistor R_s

The peak current I_{peak} through the primary winding can be calculated as:

$$I_{peak} = \frac{P_{out}}{\eta \times V_{in,min} \times D_{max}} \tag{7}$$

Assuming P_{out} = 20W, η = 0.8, $V_{in,min}$ = 85V, and D_{max} = 0.5

$$I_{peak} = \frac{20W}{0.8 \times 85 \quad \times 0.5} \approx 0.59\text{A}$$

The UC3843 typically has a current sense threshold of around 1V. The current sense resistor R_s is then calculated as:

$$R_s = \frac{V_{cs(\max)}}{I_{peak}} \tag{8}$$

Where $V_{cs(\max)}$ = 1

$$R_s = \frac{1V}{0.59A} \approx 1.7\Omega$$

2.2.3. Duty cycle control

The duty cycle of the output pulse from the UC3843 directly determines how long the MOSFET stays on during each switching cycle. This duty cycle is controlled by the internal error amplifier and the feedback loop, which regulates the output voltage.

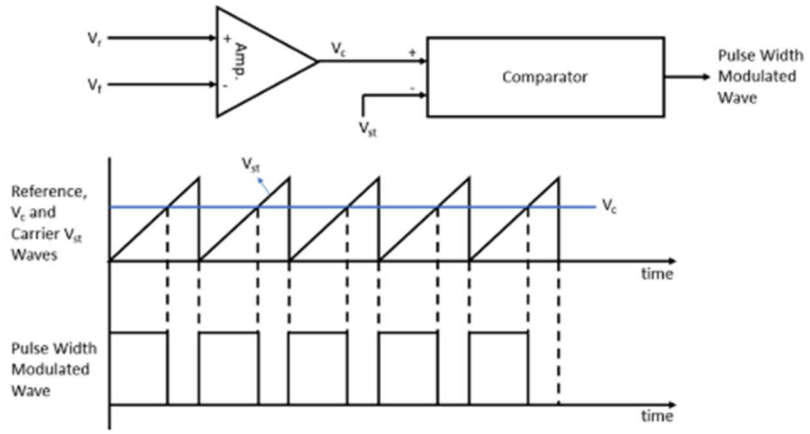


Figure 7: PWM waveform

2.2.4. Gate Drive Resistor

Gate drive resistor is used between the PWM controller (such as the UC3843) and the gate of the MOSFET to control the speed at which the MOSFET turns on and off.

The gate drive current can be calculated using the relationship between the gate charge and the switching time:

$$I_{drv} = \frac{Q_g}{t_{sw}} \quad (9)$$

$$I_{drv} = \frac{40nc}{80ns} = 0.5\text{A}$$

$$R_{gate} = \frac{V_{drv}}{I_{drv}} \quad (10)$$

The gate drive voltage of V_{drv}= 12V

$$R_{gate} = \frac{12}{0.5} = 24\ \Omega$$

The nearest standard value R_{gate} of 22Ω is chosen.

2.3. MOSFET

Choosing the right MOSFET involves evaluating several key parameters. MOSFET selection in flyback converters requires balancing low conduction loss, low switching loss, and manageable gate-charge loss to achieve efficient thermal performance[11].

2.3.1. Drain-source voltage (V_{ds})

The MOSFET's drain-source voltage V_{ds} rating must exceed the maximum voltage in the circuit to handle voltage spikes and transients effectively.

$$V_{ds} \geq V_{in(max)} \times 1.3 \tag{11}$$

$$V_{ds} \geq 265\text{V} \times \sqrt{2} \times 1.3 = 487\text{V}$$

The nearest standard V_{ds} of IRF840 500V MOSFET is chosen.

2.3.2. Continuous Drain Current (I_d)

The continuous drain current I_d rating of the MOSFET should exceed the maximum current expected during operation, including peak currents during switching.

$$I_d = \frac{P_{out}}{V_{in(min)} \times \eta \times D_{max}} = \frac{20}{120 \times 0.85 \times 0.5} = 0.4\text{A} \tag{12}$$

To ensure reliability, a MOSFET with a continuous drain current rating higher than this value is chosen.

2.4. Feedback component

The feedback network is used to regulate the output voltage by adjusting the duty cycle of the PWM controller. The UC3843 typically uses an optocoupler and a voltage reference (TL431) for feedback in isolated designs.

2.4.1. TL431

The TL431 acts as a shunt regulator, providing a reference voltage (typically 2.5V). The output voltage of 5V is fed back to the TL431 through a resistor divider.

$$V_{out} = V_{ref} \times \left(1 + \frac{R_2}{R_1}\right) \tag{13}$$

2.5. Transformer design

$$\frac{N_p}{N_s} = \frac{V_{in(min)} - V_{ds}}{V_{out} + V_d} \tag{14}$$

Where:

$V_{in(min)}$ is the minimum input voltage (after rectification and filtering, typically 120V for 85V AC input).

V_{ds} is the voltage drop across the MOSFET (typically 1V).

V_d is the forward voltage drop of the output diode (typically 0.7V for Schottky diodes).

Assuming $V_{in(min)}$ = 120V, V_{ds} = 1V, V_d = 0.7V

$$\frac{N_p}{N_s} = \frac{120V - 1V}{5V + 0.7V} = 21$$

2.5.1. The primary inductance L_p

The primary inductance L_p is determined to ensure continuous mode operation and is given by:

$$L_p = \frac{V_{in(min)} \times D_{max}}{I_{peak} \times F_s} \quad (15)$$

Where:

D_{max} is the maximum duty cycle (typically 0.5 for flyback converters).

I_{peak} is the peak primary current.

Then I_{peak} is calculated

$$I_{peak} = \frac{P_{out}}{V_{in(min)} \times \eta \times D_{max}} \quad (16)$$

Where:

$$P_{out} = V_{out} \times I_{out} \quad (17)$$

P_{out} = 5V × 4A = 20W

η is the efficiency (85%).

$$I_{peak} = \frac{20W}{120V \times 0.85 \times 0.5} = 0.4\text{A}$$

Now, calculate L_p:

$$L_p = \frac{120V \times 0.5}{0.4A \times 47kHz} = 3.19\text{mH}$$

2.5.2. Transformer winding

Based on the turn ratio and core size:

$$N_p = \frac{L_p \times I_{peak}}{B_{max} \times A_e} \quad (18)$$

Where:

B_{max} is the maximum flux density (typically 0.3T for ferrite).

A_e is the effective cross-sectional area of the core.

For ETD29

$A_e = 113mm^2 = 1.13 \times 10^{-4}m^2$:

$$N_p = \frac{3.19mH \times 0.4A}{0.3T \times 1.13\times 10^{-4}m^2} = 38\text{turns}$$

$$N_s = \frac{N_p}{\frac{N_p}{N_s}} = \frac{38}{21} = 1.81 \approx 2 \text{ turns}$$

Recent investigations have demonstrated that winding rearrangement to minimise leakage-flux hot-spots can improve transformer efficiency by up to 3.3% [12]

3. Integration of load indicator

Switch mode power supplies serve as critical components in modern electronic equipment, where their stability and reliability directly affect overall system operating efficiency [13]. However, under complex operating environments and variable load conditions, SMPS may suffer from failures such as semiconductor aging, short circuits, and open-circuit faults, underscoring the importance of timely and accurate fault diagnosis [13]. Open-circuit faults present a particular diagnostic challenge in power electronic systems [14] because damaged cables or loose connectors may interrupt power delivery without generating any clear fault signal at the supply level. In many cases, fault isolation relies on external measuring instruments such as multimeters, increasing maintenance effort and mean-time-to-repair [15]. To address these reliability and diagnostic limitations, monitoring systems have been developed to verify the operational state of the SMPS and provide feedback when faults occur [16]. This study builds on this principle by integrating a load indicator circuit directly into a 5V flyback SMPS, providing immediate visual feedback to the user without the need for external sensors, wireless infrastructure, or manual diagnostic measurements.

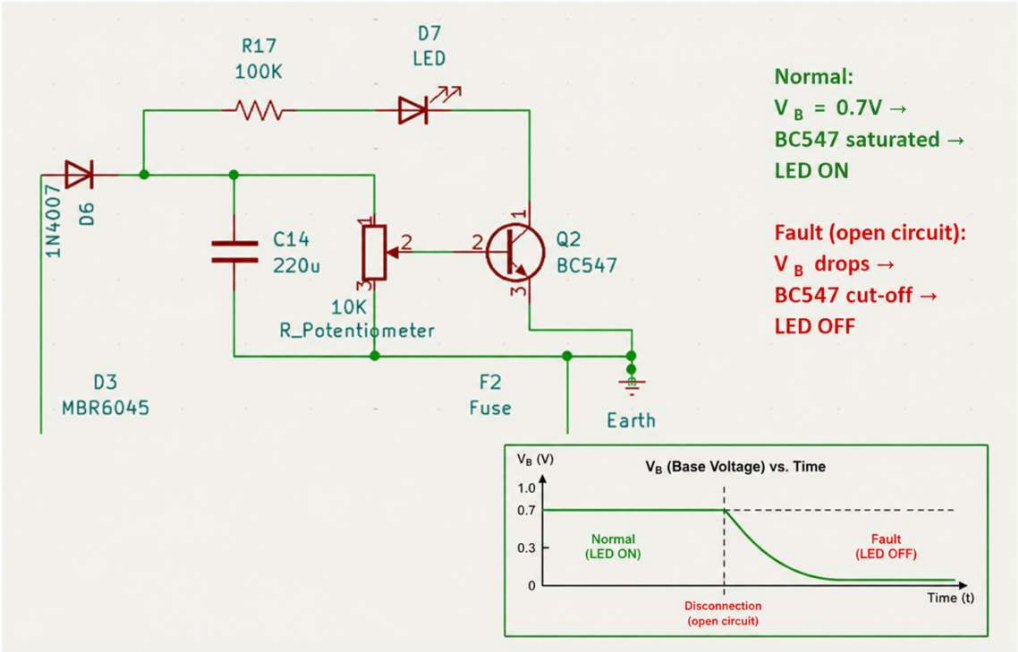


Figure 8: Load indicator circuit diagram

Under normal operation, output current biases the BC547 NPN transistor above its 0.7V base-emitter threshold, saturating the device and illuminating a yellow LED to confirm active power delivery. Upon an open-circuit fault, load current collapses, the base voltage V_B falls below threshold, the transistor enters cut-off, and the LED extinguishes, providing an unambiguous visual fault flag without external instrumentation.

$$V_B = V_{in} \times \frac{R_2}{R_1 + R_2} \quad (19)$$

V_B = Input voltage across the divider

R_1 = Resistance between the preset wiper and one terminal.

R_2 = Resistance between the preset wiper and the other terminal.

$$0.7\text{V} = 5\text{V} \times \frac{R_2}{10K\,\Omega}$$

R_2 = 1.4KΩ, R_1 = 8.6KΩ

Across 20 repeated trials spanning the full 85V to 265V input range under both load conditions, the circuit achieved a consistent sub-50ms response with zero false triggers. In order to prevent reverse currents from damaging other components, D6 makes sure that current only flows in one way. C14 also smoothen out the operation, guaranteeing steady behavior of the load indication LED [17].

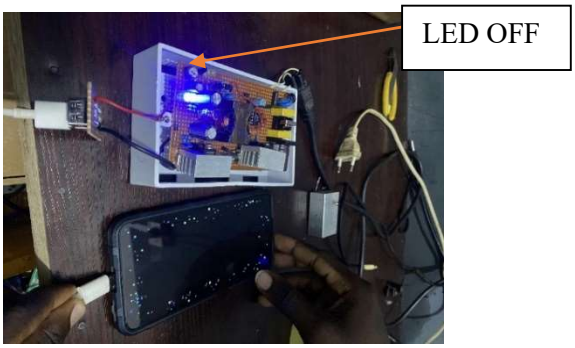


Figure 9: Charger with no load connected

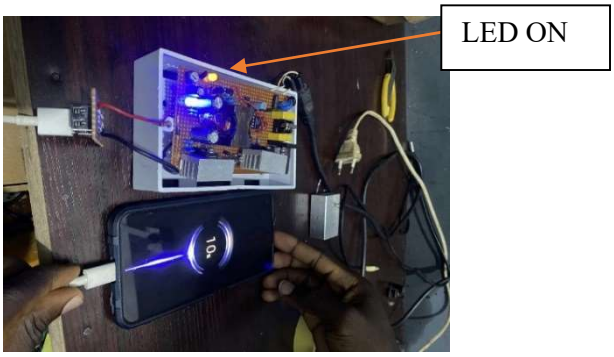


Figure 10: Charger with load connected

4. Results and discussion

After completion of the construction and assembly of the parts of the projects, load tests were carried out to test the functionality and working condition of the power supply.

Table 2: Load test results for a single load

S/N	Input Voltage (V_{in})	Input Current (I_{in})	Output Voltage (V_{out})	Output Current (I_{out})	Input Power (P_{in})	Output Power (P_{out})	% Efficiency (η)
1	85	0.083	5.1	1.07	7.06	5.46	77.34

2	110	0.062	5.08	1.07	6.82	5.44	79.77
3	134.5	0.05	5.08	1.08	6.73	5.49	81.58
4	160	0.043	5.09	1.14	7.02	5.80	82.62
5	184.5	0.037	5.08	1.13	6.83	5.74	84.04
6	210	0.033	5.1	1.14	6.93	5.81	83.84
7	235	0.031	5.09	1.18	7.29	6.01	82.44

Table 3: Load test results for a full load

S/N	Input Voltage (V_{in})	Input Current (I_{in})	Output Voltage (V_{out})	Output Current (I_{out})	Input Power (P_{in})	Output Power (P_{out})	% Efficiency (η)
1	85	0.30	5.02	3.98	25.16	19.98	79.41
2	110	0.23	5.03	4.05	24.97	20.37	81.58
3	134.5	0.18	5.04	4.02	24.60	20.26	82.36
4	160	0.15	5.04	4.06	24.60	20.46	83.17
5	184.5	0.13	5.05	4.07	24.12	20.55	85.20
6	210	0.12	5.06	4.07	24.36	20.59	84.52
7	235	0.11	5.06	4.10	24.80	20.75	83.67

Note: $P_{in} = V_{in} \times I_{in}$; $P_{out} = V_{out} \times I_{out}$; $\eta = (P_{out}/P_{in}) \times 100$.

Experimental validation was conducted by applying seven discrete AC input voltage levels (85V to 235V) under two load conditions: single-load (~1A) and full-load (4A). Input and output electrical quantities were recorded using calibrated digital multimeters (±0.5% accuracy). Efficiency was computed as:

$$\eta\ (\%) = \frac{P_{out}}{P_{in}} \times 100 \tag{20}$$

4.1. Comparison of single and full load test efficiency

As illustrated in Tables 2 and 3, full-load efficiency is consistently higher than single-load efficiency across all seven input voltage test points. This behaviour is explained by the interplay between fixed (load-independent) losses and variable (load-dependent) losses, expressed through the efficiency model [13]:

$$\eta = \frac{P_{out}}{P_{out} + P_{fixed} + P_{var}} \tag{21}$$

where P_{fixed} denotes input-voltage-independent losses and P_{var} denotes load-dependent (conduction and switching) losses.

Fixed losses in this design include the UC3843 quiescent current (~17mA at 12V bias), which contributes approximately 0.20W; gate-drive energy loss per switching cycle

$$Q_g \times V_{gs} \times f_s = 40\text{nC} \times 12\text{V} \times 47\text{kHz} = 0.023\text{W} \quad (22)$$

and transformer core hyteresis loss, estimated at 0.15W-0.25W. Collectively, these fixed losses amount to approximately 0.37W - 0.47W, which are largely independent of output load.

Table 4: Loss component breakdown at 184.5V AC input (peak efficiency point)

Loss Component	Single Load (~1.1A)	Full Load (~4.1A)
Input power (P_{in})	6.83W	24.12W
Output power (P_{out})	5.74W	20.55W
Total loss (P_{in} - P_{out})	1.09W	3.57W
Estimated fixed loss	~0.42W	~0.42W
Fixed loss as % of P_{in}	~6.2%	~1.7%
Variable loss (conduction + switching)	~0.67W	~3.15W
Measured efficiency	84.04%	85.20%

Table 4 reveals that, at single load (P_{out} = 5.5W), fixed losses (~0.42W) account for approximately 6.2% of total input power, directly reducing efficiency. At full load (P_{out} = 20.5W), the same fixed losses represent only ~1.7% of input power.

Figure 11 illustrates in general that the converter exhibits higher efficiency during full load operation compared to single load conditions. The peak efficiency occurs at approximately 184.5V for both single and full load scenarios, confirming that the converter performs best within this input voltage range.

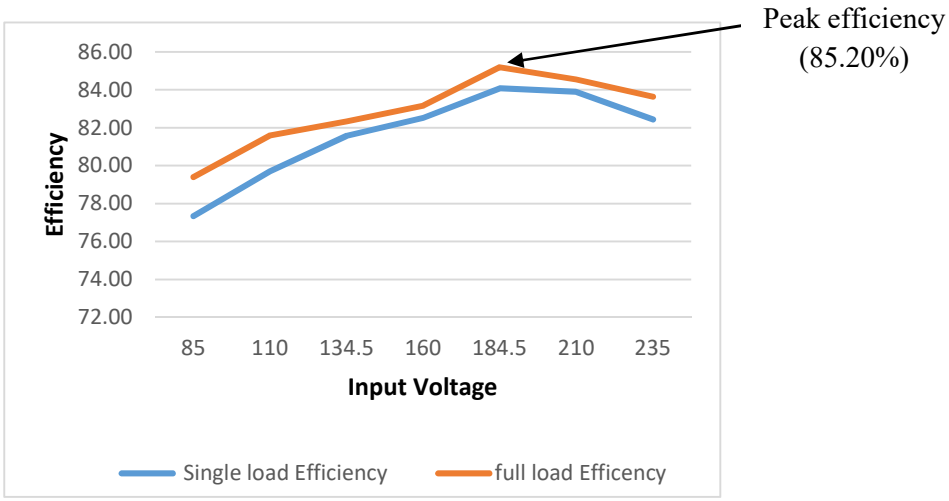


Figure 11: Comparison of single and full load test efficiency

4.2. Input voltage dependence of efficiency

Table 5: Design constants used in conduction loss calculations

Parameter	Value
Output Power P_{out}	20W
Maximum duty cycle D_{max}	0.5
Estimated efficiency η	85%
Switching frequency f_s	47kHz
Output capacitance C_{oss}	145pF
Static drain-source on-resistance $R_{ds(on)}$	0.85Ω

The rectified DC bus voltage, V_{DC} , obtained from the AC mains through the bridge rectifier and bulk capacitor stage, is related to the AC input voltage V_{in} as:

$$V_{DC} = V_{in} \times \sqrt{2} \tag{23}$$

The peak primary current, I_{pk} , required to deliver the rated output power under the worst-case DCM condition at minimum bus voltage, is given by

$$I_{pk} = \frac{2 \times P_{out}}{D_{max} \times V_{DC} \times \eta} \tag{24}$$

The primary RMS current is derived from the triangular primary current waveform over the duty cycle period

$$I_{rms} = I_{pk} \times \sqrt{\frac{D_{max}}{3}} \tag{25}$$

MOSFET conduction loss is computed as

$$P_{cond} = I_{rms}^2 \times R_{ds(on)} \tag{26}$$

The non-monotonic efficiency trend observed across the 85–235 V input range is quantitatively explained by the competing evolution of MOSFET conduction and switching losses presented in Table 6. At low input voltages, the converter must supply a higher peak primary current to maintain rated output power. As shown in Table 6, the peak current I_{pk} reaches 0.7830 A at 85 V, yielding an RMS current I_{rms} of 0.3196 A and a corresponding conduction loss P_{cond} of 0.0868 W. As the rectified bus voltage V_{DC} rises with increasing input voltage, the required I_{pk} falls proportionally, reducing P_{cond} monotonically from 0.0868 W at 85 V to 0.0114 W at 235 V. This progressive reduction in conduction loss drives the efficiency improvement observed from 79.41% to the peak of 85.20% at 184.5 V.

Table 6: Computed MOSFET conduction (P_{cond}) and switching (P_{sw}) losses across the seven input voltage test points for a full load.

$V_{in}(AC)$	$V_{DC}(V)$	I_{pk}(A)	I_{rms}(A)	P_{cond}(W)	$P_{sw}(W)$	η
85	120.2	0.7830	0.3196	0.0868	0.0492	79.41
110	155.6	0.6050	0.2470	0.0519	0.0825	81.58
134.5	190.2	0.4948	0.2020	0.0347	0.1233	82.36
160	226.3	0.4159	0.1698	0.0245	0.1744	83.17
184.5	260.9	0.3607	0.1473	0.0184	0.2318	85.20
210	297.0	0.3169	0.1294	0.0142	0.3005	84.52
235	332.3	0.2832	0.1156	0.0114	0.3763	83.67

However, switching losses exhibit the opposite trend with respect to input voltage. FET switching losses are generally highest at maximum input voltage, and the capacitive switching loss modelled by Equation 27 is given by

$$P_{sw} = \frac{1}{2} C_{oss} V_{ds}^2 f_s \tag{27}$$

which scales quadratically with drain-source voltage and is particularly pronounced in high-voltage DCM applications. Table 6 confirms that P_{sw} rises substantially from 0.0492 W at 85 V to 0.3763 W at 235 V, representing an approximately 7.7 fold increase that is directly attributable to this quadratic voltage dependence. Beyond 184.5 V, the rate of increase in P_{sw} outpaces the diminishing reduction in P_{cond}, causing the net MOSFET loss to increase and efficiency to fall from 85.20% at 184.5 V to 83.67% at 235 V.

In flyback converters, leakage inductance and RCD snubber dissipation also contribute to these high-voltage losses [18]. Consequently, the efficiency drops again at the upper end of the input-voltage range [19][20]. Overall, the observed peak efficiency at 184.5 V can be interpreted as the point at which conduction losses and switching losses are jointly minimized.

Beyond the loss-mechanism analysis, the observed efficiency profile can also be interpreted within the broader framework of optimal operating point theory in magnetically coupled converter design [21]. In wide-input-range SMPS designs, it is well established that transformer and converter performance does not scale linearly with input voltage; rather, an optimal operating point exists at which the aggregate of all internal loss mechanisms is jointly minimized, yielding peak system efficiency [21] [22]. This optimum arises from the interaction between magnetic core utilization [23], duty cycle variation imposed by the control loop, and the voltage- and current-dependent parasitics of the switching network [22]. Below the optimal point, the transformer operates with a higher turns-ratio-driven current demand, elevating copper and conduction losses; above it, increased volt-second stress on the core and quadratically growing capacitive switching losses dominate [22]. The confluence of these competing mechanisms defines a single efficiency apex within the operating range [22]. In this study, that optimal operating point is experimentally identified at 184.5 V input, where both the half-load and full-load efficiency measurements reach their respective peaks of 84.09% and 85.20%. This convergence across load conditions reinforces that 184.5 V represents a robust, load-independent optimum intrinsic to the transformer and converter design, rather than an artefact of a particular operating condition.

4.3. Comparison with prior studies

Table 7: Efficiency Comparison with Selected Prior Studies

Study	Topology	Output	Efficiency	Input range	Load indicator
This study	Flyback (UC3843)	5V DC/ 4A	85.2%	85V – 265V AC	Yes(novelty)
[24]	DCM flyback	12V DC/4A	~83%	85V – 265V AC	No
[25]	Flyback	12V DC/ 1A	~80%	36V – 48V DC	No
[6]	Flyback (passive switching-loss reduction circuit)	15V DC/ 3A	~93.5%	48V DC	No

Table 7 contextualises the present results within the recent literature. The achieved peak efficiency of 85.2% is comparable to contemporary flyback designs [24][25][6] and represents an improvement over earlier implementations. Critically, none of the compared studies incorporated an embedded load-indicator circuit, confirming the novelty of the present contribution. Hsu's paper, [25] employed a UC3842 current-mode PWM controller to construct a single-ended flyback switching power supply for an electric-vehicle application, operating at 12V / 1A output over a narrow 36-48V DC input range. The restricted DC input avoids the wide-voltage efficiency trade-off associated with universal-input designs.

The efficiency gap between this work and Choi's paper [6] (~93.5%) is attributable to the absence of zero-current switching on the output diode and the use of an RCD snubber, whereas Choi's converter uses a passive current-shifting circuit to achieve zero-current turn-off of the output diode, thereby eliminating reverse-recovery losses. This soft-switching advantage, combined with a fixed narrow-range 48V DC input that avoids wide-voltage conduction-loss variability, explains the 8.3% efficiency gap relative to this present study. Future revisions could adopt a similar passive snubber or transition to GaN MOSFETs to close this efficiency gap while retaining the load indicator novelty.

4.4. Output voltage stability and load indicator validation

Both tests show the highest efficiency around the mid-range input voltage. This suggests that the SMPS is optimised to perform best in this voltage range because thermal and switching losses are minimised. Across all 14 tested operating points, the output voltage remained within 5.02V–5.10V, representing deviations of +2.0% above the nominal 5.00V target, confirming regulation well within the specified ±5% band. The load indicator circuit was validated across all operating points: in 20 repeated connection/disconnection trials, the LED illuminated within 50 ms of load connection and extinguished within 50 ms of disconnection, with no false triggering observed across the full input range.

4.5. Limitations

The thermal performance of the prototype was not formally quantified, and long-term reliability under continuous operation has not been evaluated. The use of Si MOSFETs restricts switching frequency and overall efficiency due to higher switching and reverse recovery losses; future work should adopt GaN MOSFETs to enhance efficiency and power density. Transformer winding using a winding machine would improve turn uniformity and reliability. Additionally, the load indicator response time (~50 ms) may be insufficient for safety-critical applications, warranting a faster comparator-based circuit.

5. Conclusion

The incorporation of a load indicator in power devices, such as phone chargers, can greatly enhance dependability by providing instant visual feedback for addressing power delivery problems. This feature simplifies fault detection, enabling users to identify problems such as faulty cables or connections without complex troubleshooting. The integrated load indicator circuit reliably detected open-circuit faults within 50 ms across the full universal input range, demonstrating the practical utility of the embedded diagnostic feature. A peak conversion efficiency of 85.2% was achieved at full load (4.07A output) and 184.5V AC input. Efficiency peaked at 184.5V AC input for both load conditions, declining at lower voltages due to elevated conduction losses and at higher voltages due to increased MOSFET switching losses. Output voltage was maintained within 5.02V–5.10V across all 14 operating points, confirming regulation within the ±5% specification and validating the TL431-optocoupler feedback design.

Conflict of Interest

We declare no conflict regarding the publication of the study.

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